



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/626,086	07/24/2003	Timothy Roy Block	ROC920030026US1	9970
30206	7590	12/09/2008	EXAMINER	
IBM CORPORATION			NGUYEN, THUONG	
ROCHESTER IP LAW DEPT. 917				
3605 HIGHWAY 52 NORTH			ART UNIT	PAPER NUMBER
ROCHESTER, MN 55901-7829			2455	
			MAIL DATE	DELIVERY MODE
			12/09/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte TIMOTHY ROY BLOCK,
BOB RICHARD CERNOHOUS, and
JOHN CHRISTIAN UNTERHOLZNER

Appeal 2008-0853
Application 10/626,086
Technology Center 2400

Decided: December 9, 2008

Before JOSEPH L. DIXON, ST. JOHN COURTENAY III, and
THU A. DANG, *Administrative Patent Judges*.
COURTENAY, *Administrative Patent Judge*.

DECISION ON APPEAL

This is a decision on appeal under 35 U.S.C. § 134(a) from the Examiner's rejection of claims 1, 3-16, and 18-36. Claims 2 and 17 are cancelled. We have jurisdiction under 35 U.S.C. § 6(b).

We REVERSE.

THE INVENTION

The disclosed invention relates generally to cluster computer systems. More particularly, the present invention relates to data transfer between nodes in clustered computer systems. (Spec. 1, ll. 5-6).

Independent claim 1 is illustrative:

1. A method of communicating between a source and a target node in a clustered computer system, the method comprising:

establishing a cluster data port between the source node and a target node, the cluster data port configured to select among a plurality of connection paths between the source node and the target node, and to selectively switch over data flow from the target node to a backup target node, wherein establishing the cluster data port includes establishing multiple concurrent logical connections between the source node and the target node, each logical connection configured to communicate data over a connection path among the plurality of connection paths; and;

communicating data from the source node to the target node using the cluster data port.

THE REFERENCES

The Examiner relies upon the following references as evidence in support of the rejections:

1. Modi. US 6,587,866 B1 Jul. 1, 2003
(filed Jan. 10, 2000)
2. Foster US 2002/0161923 A1 Oct. 31, 2002
(filed Oct. 26, 2001)

THE REJECTIONS

1. The Examiner rejected claims 1, 16, 31, and 35 under 35 U.S.C. § 112, first paragraph.
2. The Examiner rejected claims 1, 16, 31, and 35 under 35 U.S.C. § 112, second paragraph.
3. The Examiner rejected claims 1-4, 6, 8-10, 12, 14-19, 21, 23-25, 27, and 29-36 under 35 U.S.C. § 102(e) as being anticipated by Foster.
4. The Examiner rejected claims 5, 7, 11, 13, 20, 22, 26, and 28 under 35 U.S.C. § 103(a) as being obvious over Foster in view of Modi.

Appellants have the burden on appeal to the Board to demonstrate error in the Examiner's position. *See In re Kahn*, 441 F.3d 977, 985-86 (Fed. Cir. 2006). Therefore, we look to Appellants' Brief to show error in the proffered *prima facie* case.

35 U.S.C. § 112, first paragraph

ISSUE

Did the Examiner err in rejecting claims 1, 16, 31 and 35 under 35 U.S.C. § 112, first paragraph as failing to comply with the written description requirement? In particular, have Appellants shown that the Examiner erred in determining that the original disclosure did not disclose "concurrent logical connections?"

PRINCIPLES OF LAW

35 U.S.C. § 112, first paragraph

To satisfy the written description requirement, a patent Specification must describe the claimed invention in sufficient detail that one skilled in the art can reasonably conclude that the inventor had possession of the claimed invention. *See, e.g., Moba, B.V. v. Diamond Automation, Inc.*, 325 F.3d 1306, 1319, (Fed. Cir. 2003); *Vas-Cath, Inc. v. Mahurkar*, 935 F.2d 1555 1563. However, a showing of possession alone does not cure the lack of a written description. *Enzo Biochem, Inc. v. Gen-Probe, Inc.*, 323 F.3d 956, 969 (Fed. Cir. 2002). Much of the written description case law addresses whether the Specification as originally filed supports claims not originally in the application.

ANALYSIS

Appellants contend that the Examiner erred in rejecting independent claims 1, 16, 31, and 35 because the Specification as a whole would be interpreted by one of ordinary skill in the art as teaching that the multiple logical connections established between two nodes are concurrent logical connections.

Fig. 1 of Appellants' disclosure shows multiple, parallel connection paths 20 between nodes 12 and 14. In addition, the Specification teaches providing multiple connection paths 22 from a node 12 . . . to network 18, and also that multiple logical connections may be made between any pairs of nodes. (Spec. p. 6, l. 27 – p. 7 l. 7). Thus, the question is whether the parallel

connection paths would be interpreted as being “concurrent” by one skilled in the art. As admitted by Appellants, “*concurrent* logical connections” are not explicitly mentioned in the disclosure (App. Br. 5, ¶2).

As discussed by the Appellants, the plain meaning of the term “concurrent” is “happening at the same time as something else.” (App. Br. 5). Therefore, as matter of interpretation, Appellants’ disclosure must show to one skilled in the art that the multiple logical connections between a pair of nodes occur at the same time.

Fig. 1 shows multiple logical connection paths between nodes 12 and 14 that do in fact occur at the same time, i.e., concurrent. Further, we agree with Appellants’ argument that load balancing over multiple logical connections between two nodes involves the communication of data over the logical connections in parallel to improve the overall data throughput between the two nodes. In order to have parallel connections, these connections must occur at the same time.

Based on the above, we agree with Appellants that as a question of fact, Appellants’ disclosure would have been interpreted by one of ordinary skill in the art as teaching that the multiple logical connections established between two nodes are concurrent logical connections, as claimed. Thus, we reverse the Examiner’s rejection of claims 1, 16, 31, and 35 under 35 U.S.C. § 112, first paragraph as failing to comply with the written description requirement.

35 U.S.C. § 112, second paragraph

ISSUE

Did the Examiner err in rejecting claims 1, 16, 31, and 35 under 35 U.S.C. § 112, second paragraph as failing to comply with the written description requirement because the original disclosure did not disclose “concurrent logical connections?”

PRINCIPLES OF LAW

35 U.S.C. §112, second paragraph

The Specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

There are two separate requirements set forth in this paragraph:

- (A) the claims must set forth the subject matter that applicants regard as their invention; and
- (B) the claims must particularly point out and distinctly define the metes and bounds of the subject matter that will be protected by the patent grant.

The first requirement is a subjective requirement because it is dependent on what the applicants for a patent regard as their invention. The second requirement is an objective requirement because it is not dependent on the views of applicant or any particular individual, but is evaluated in the context of whether the claim is definite - i.e., whether the scope of the claim is clear to a hypothetical person possessing the ordinary level of skill in the pertinent art.

The inquiry during examination is patentability of the invention as applicant regards it. If the claims do not particularly point out and distinctly claim that which applicants regard as their invention, the appropriate action by the examiner is to reject the claims under 35 U.S.C. 112, second paragraph. *In re Zletz*, 893 F.2d 319 (Fed. Cir. 1989).

ANALYSIS

Appellants contend that the Examiner erred in rejecting claims 1, 16, 31, and 35 under § 112, second paragraph. Appellants contend that as previously discussed in regards to the rejection under § 112, first paragraph, that the element “concurrent logical connections” is well-supported in the Specification. Thus, Appellants conclude that claims 1, 16, 31, and 35 are also compliant with the requirements of 35 U.S.C. § 112 second paragraph.

As discussed *supra*, we determined that the element “concurrent logical connections” is supported in the Specification. Thus, it is our view that this element is also definite and distinctly claimed in claims 1, 16, 31, and 35 under § 112, second paragraph.

Accordingly, we reverse the Examiner’s rejection of independent claims 1, 16, 31, and 35 under 35 U.S.C. § 112, second paragraph.

Anticipation under 35 U.S.C. § 102

Claims 1-4, 6, 8-10, 12, 14-19, 21, 23-25, 27, and 29-36

ISSUE

Did the Examiner err in rejecting claims 1-4, 6, 8-10, 12, 14-19, 21, 23-25, 27, and 29-36 because the claimed element “establishing multiple

concurrent logical connections between a pair of nodes” is purportedly not supported in the Specification?

PRINCIPLES OF LAW

In rejecting claims under 35 U.S.C. § 102, “[a] single prior art reference that discloses, either expressly or inherently, each limitation of a claim invalidates that claim by anticipation.” *Perricone v. Medicis Pharm. Corp.*, 432 F.3d 1368, 1375-76 (Fed. Cir. 2005) (citation omitted). “Anticipation of a patent claim requires a finding that the claim at issue ‘reads on’ a prior art reference.” *Atlas Powder Co. v. IRECO, Inc.*, 190 F.3d 1342, 1346 (Fed Cir. 1999) (“In other words, if granting patent protection on the disputed claim would allow the patentee to exclude the public from practicing the prior art, then that claim is anticipated, regardless of whether it also covers subject matter not in the prior art.”) (Internal citations omitted.)

FINDINGS OF FACT

1. Foster teaches identifying and configuring new paths, and assigning new paths to virtual addresses. (Foster, p. 3).

ANALYSIS

We consider the Examiner’s rejection of claims 1-4, 6, 8-10, 12, 14-19, 21, 23-25, 27, and 29-36 under 35 U.S.C. § 102(e) as being anticipated by Foster.

Appellants contend that Foster fails to teach the element of multiple concurrent logical connections, as recited in claim 1. We agree for the reasons discussed *infra*.

Foster teaches identifying and configuring new paths, and assigning new paths to virtual addresses. (FF 1). However, we agree with Appellants that Foster teaches establishing only one path at a time for a particular virtual address used by a source node. Thus, we find Appellants' arguments persuasive that Foster teaches that a virtual address is associated at any time with only a single path, as opposed to the multiple paths required by the independent claims.

The Examiner asserted that Appellants' arguments regarding this element are invalid because the element is not supported in the Specification. However, a rejection under 35 U.S.C. § 112, first paragraph does not absolve the Examiner from having to present a prior art showing that meets all of the criteria of anticipation, i.e., that all of the claimed limitations must be taught by a single reference.

The Examiner asserted that Foster discloses the method of checking to see if all ports are selected or connected. Therefore, the connections could be connected one after another, or could be established at the same time. (Ans. p. 18). However, mere probabilities or possibilities are not enough to establish *prima facie* anticipation under 35 U.S.C. § 102. "Inherency ... may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient."

In re Robertson, 169 F.3d 743, 745 (Fed. Cir. 1999)

Based on the record before us, we conclude that Foster fails to disclose the limitation of multiple concurrent logical connections, as recited in independent claims 1, 16, 31, and 35. Thus, Appellants have shown that the Examiner erred in rejecting independent claims 1, 16, 31, and 35 and corresponding dependent claims. Accordingly, we reverse the Examiner's rejection of claims 1-4, 6, 8-10, 12, 14-19, 21, 23-25, 27, and 29-36 under 35 U.S.C. § 102(e) as being anticipated by Foster.

Obviousness under 35 U.S.C. § 103
Claims 5, 7, 11, 13, 20, 22, 26, and 28

We next consider the Examiner's rejection of claims 5, 7, 11, 13, 20, 22, 26, and 28 under 35 U.S.C. § 103(a) as being unpatentable over Foster in view of Modi.

As discussed above, we find that Foster fails to teach the element of multiple concurrent logical connections as recited in independent claims 1 and 16, from which claims 5, 7, 11, 13, 20, 22, 26, and 28 depend.

We do not find, nor does the Examiner establish, that Modi cures the deficiencies of Foster that were discussed above. Thus, for this reason, we also reverse the Examiner's rejection of claims 5, 7, 11, 13, 20, 22, 26, and 28 under 35 U.S.C. §103(a) as being unpatentable over Foster in view of Modi.

CONCLUSIONS OF LAW

Based on the findings of facts and analysis above, we conclude the following:

The Examiner erred in determining that the claimed “multiple concurrent logical connections” was not supported by the written description.

The Examiner erred in determining that claimed element “multiple concurrent logical connections” was indefinite.

The Examiner erred in determining that Foster teaches the limitations of claims 1-4, 6, 8-10, 12, 14-19, 21, 23-25, 27, and 29-36.

The Examiner erred in determining that the combination of Foster and Modi teaches or fairly suggests the limitations of claims 5, 7, 11, 13, 20, 22, 26, and 28.

Based on the findings of facts and analysis above, we conclude that Appellants have met their burden of showing that the Examiner erred in rejecting claims 1, 16, 31, and 35 under 35 U.S.C. § 112, first paragraph as failing to comply with the written description requirement.

Based on the findings of facts and analysis above, we conclude that Appellants have met their burden of showing that the Examiner erred in rejecting claims 1, 16, 31, and 35 under 35 U.S.C. § 112, second paragraph for being indefinite.

Based on the findings of facts and analysis above, we conclude that Appellants have met their burden of showing that the Examiner erred in rejecting claims 1-4, 6, 8-10, 12, 14-19, 21, 23-25, 27, and 29-36 as being anticipated by Foster under 35 U.S.C. § 102(e).

Appeal 2008-0853
Application 10/626,086

Based on the findings of facts and analysis above, we conclude that Appellants have met their burden of showing that the Examiner erred in rejecting claims 5, 7, 11, 13, 20, 22, 26, and 28 as being unpatentable over Foster in view of Modi under 35 U.S.C. § 103(a).

DECISION

The decision of the Examiner rejecting claims 1, 3-16, and 18-36 is reversed.

REVERSED

pgc

IBM CORPORATION
ROCHESTER IP LAW DEPT. 917
3605 HIGHWAY 52 NORTH
ROCHESTER MN 55901-7829